AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A semiconductor wafer protection structure, comprising a semiconductor wafer and a protective sheet overlaid on a circuit surface of the semiconductor wafer, wherein the protective sheet has a larger diameter than the outer diameter of the semiconductor wafer.

2. (Original) A semiconductor wafer protection structure, comprising a semiconductor wafer and a laminated protective sheet overlaid on a circuit surface of the semiconductor wafer, wherein the laminated protective sheet comprises a first protective layer having substantially the same size as the outer diameter of the semiconductor wafer and a second protective layer laminated on the first protective layer and having an outer diameter that is equal to or larger than the outer diameter of the first protective layer, and the laminated protective sheet is overlaid on the circuit surface via the side of the first protective layer.

3. (Currently Amended) The semiconductor wafer protection structure according to claim 1 ~~or 2~~, wherein the protective sheet or the laminated protective sheet has a maximum diameter that is larger than the outer diameter of the semiconductor wafer by +0.1 to 10 mm.

4. (Original) The semiconductor wafer protection structure according to claim 2, wherein the first protective layer has an outer diameter that is smaller than the outer diameter of the semiconductor wafer by -2.0 to 0 mm and the second protective layer has an outer diameter that is larger than the outer diameter of the semiconductor wafer by +0.1 to +2.0 mm.

5. (Currently Amended) The semiconductor wafer protection structure according to claim 2 ~~or 4~~, wherein the first protective layer includes a film having a stress relaxation rate of at least 40% after 1 minute of 10% elongation, and the second protective layer includes a film having a value of Young's modulus x thickness of at least 5.0×10^4 N/m.

6. (Original) A semiconductor wafer protection method, comprising overlaying a circuit surface of a semiconductor wafer with a protective sheet having a larger diameter than the outer diameter of the semiconductor wafer.

7. (Original) A semiconductor wafer protection method, comprising overlaying a circuit surface of a semiconductor wafer with a laminated protective sheet, wherein the laminated protective sheet comprises a first protective layer having substantially the same size as the outer diameter of the semiconductor wafer and a second protective layer laminated on the first protective layer and having an outer diameter that is equal to or larger than the outer diameter of the first protective layer, and the laminated protective sheet is overlaid on the circuit surface via the side of the first protective layer.

8. (Currently Amended) The semiconductor wafer protection method according to claim 6 ~~or 7~~, wherein the protective sheet or the laminated protective sheet has a maximum diameter that is larger than the outer diameter of the semiconductor wafer by +0.1 to 10 mm.

9. (Original) The semiconductor wafer protection method according to claim 7, wherein the first protective layer has an outer diameter that is smaller than the outer diameter of the semiconductor wafer by -2.0 to 0 mm and the second protective layer has an outer diameter that is larger than the outer diameter of the semiconductor wafer by +0.1 to +2.0 mm.

10. (Currently Amended) The semiconductor wafer protection method according to claim 7 ~~or 9~~, wherein the first protective layer includes a film having a stress relaxation rate of at least 40% after 1 minute of 10% elongation, and the second protective layer includes a film having a value of Young's modulus x thickness of at least 5.0×10^4 N/m.

11. (Original) A laminated protective sheet for semiconductor wafer comprising a first protective layer and a second protective layer, wherein the second protective layer has a larger outer diameter than that of the first protective layer.

12. (Original) The laminated protective sheet for semiconductor wafer according to claim 11, wherein the second protective layer has an outer diameter that is larger than the outer diameter of the first protective layer by +0.1 to +4.0 mm.

13. (Currently Amended) The laminated protective sheet for semiconductor wafer according to claim 11 ~~or 12~~, wherein the first protective layer includes a film having a stress relaxation rate of at least 40% after 1 minute of 10% elongation, and the second protective layer includes a film having a value of Young's modulus x thickness of at least $5.0x10^4$ N/m.

14. (Currently Amended) A process for processing a semiconductor wafer, comprising a step comprising backgrinding a semiconductor wafer and applying an adhesive sheet to the ground surface while protecting the semiconductor wafer by the semiconductor wafer protection method of ~~any one of claims 6 to 10~~claim 6.

15. (Original) The process for processing a semiconductor wafer according to claim 14, comprising a further step comprising cutting off an outer peripheral portion of the adhesive sheet with a cutter in a manner such that the cutter is moved along an outer peripheral end surface of the protective sheet or the laminated protective sheet.

16. (New) The semiconductor wafer protection structure according to claim 2, wherein the protective sheet or the laminated protective sheet has a maximum diameter that is larger than the outer diameter of the semiconductor wafer by +0.1 to 10 mm.

17. (New) The semiconductor wafer protection structure according to claim 4, wherein the first protective layer includes a film having a stress relaxation rate of at least

40% after 1 minute of 10% elongation, and the second protective layer includes a film having a value of Young's modulus x thickness of at least $5.0x10^4$ N/m.

18. (New) The semiconductor wafer protection method according to claim 7, wherein the protective sheet or the laminated protective sheet has a maximum diameter that is larger than the outer diameter of the semiconductor wafer by +0.1 to 10 mm.

19. (New) The semiconductor wafer protection method according to claim 9, wherein the first protective layer includes a film having a stress relaxation rate of at least 40% after 1 minute of 10% elongation, and the second protective layer includes a film having a value of Young's modulus x thickness of at least $5.0x10^4$ N/m.

20. (New) The laminated protective sheet for semiconductor wafer according to claim 12, wherein the first protective layer includes a film having a stress relaxation rate of at least 40% after 1 minute of 10% elongation, and the second protective layer includes a film having a value of Young's modulus x thickness of at least $5.0x10^4$ N/m.